AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-20 (canceled). The patent is a divisional. Claims 1-20 were allowed (see U.S. Patent 6,335,249 B1).

Claim 21 (previously presented)

A Salicide field effect transistor with improved borderless contact openings comprised of:

a semiconductor substrate doped with a first conductive type dopant and having device areas surrounded and electrically isolated by shallow trench field oxide areas;

a gate oxide layer on said device areas, and a conductively doped patterned polysilicon layer doped with a second conductive type dopant over said device areas for gate electrodes;

lightly doped source/drain areas with said second conductive type dopant in said device areas adjacent to said gate electrodes and insulating sidewall spacers on the sidewalls of said gate electrodes;

heavily doped first source/drain contact areas composed of said second conductive type dopant in said device areas adjacent to said insulating sidewall spacers;

a silicide layer on said gate electrodes and on

said source/drain contact providing said Salicide field effect transistors;

a conformal barrier layer, and an interlevel dielectric layer on said Salicide field effect transistor;

borderless contact openings in said interlevel dielectric layer and said barrier layer to said source/drain areas and extending over said field oxide with unintentional over-etched field oxide regions at said field oxide-source/drain area interface;

a dopant composed of said second conductive type in said substrate under and adjacent to said over-etched field oxide regions in said borderless contact openings and providing said source/drain contact areas with a conformal continuous ion implanted doped region in said substrate surrounding said unintentional over-etched field oxide regions, and said ion implanted doped region is shallower than said source/drain contact areas.

Claims 22-25 (original)

22. The structure of claim 21, wherein said semiconductor substrate is single crystal silicon.

23. The structure of claim 21, wherein said silicide layer is titanium silicide.

24. The structure of claim 21, wherein said silicide layer is cobalt silicide.

25. The structure of claim 21, wherein said first conductive type dopant is a P-type dopant and said second type dopant is an N-type dopant for Salicide N-channel FETs, and the dopant types are reversed for P-channel salicide FETs.